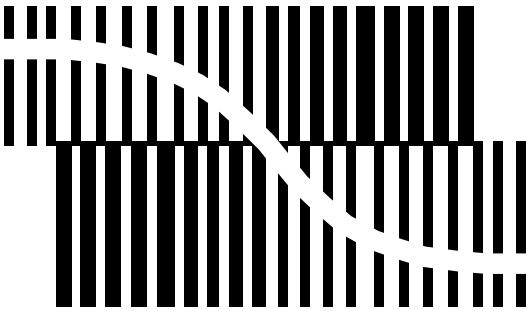
DATA SHEET



SAA7367
Bitstream conversion ADC for digital audio systems

Objective specification
File under Integrated Circuits, IC01

1996 Jun 17

Philips
Semiconductors

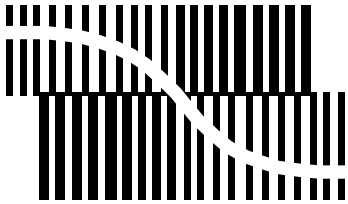
PHILIPS

Bitstream conversion ADC for digital audio systems

SAA7367

FEATURES

- Total Harmonic Distortion plus Noise (THD + N) = –88 dB (0.004%); DR = 93 dB; S/N = 97 dB
- Simple interfacing to analog inputs
- Small, non-critical PCB layout
- Low pin-out SO24 package (pin-compatible to SAA7366)
- 4 flexible serial interface modes
- 4.5 to 5.5 V operation
- Standby mode
- Detection of digital signal ≥–1 dB amplitude
- Up to 18 significant bits serial output
- Selectable high-pass filter.



BITSTREAM CONVERSION

GENERAL DESCRIPTION

The SAA7367 is a CMOS low-cost stereo Analog-to-Digital Converter (ADC) using the Philips bitstream conversion technique.

APPLICATIONS

The device is designed for the digital acquisition of analog audio signals for digital audio systems such as:

- Compact Disc-Recordable (CD-R)
- Digital Compact Cassette (DCC)
- Digital Audio Tape (DAT).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDD}	digital supply current		–	17	–	mA
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current		–	13	–	mA
f_{BCK}	clock input frequency		4.60	12.288	12.8	MHz
f_s	sample rate		18	48	50	kHz
THD + N	total harmonic distortion plus noise	at 0 dB input	–	–88	–80	dB
DR	dynamic range	at –60 dB	90	93	–	dB
S/N	signal-to-noise ratio		–	97	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7367	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

BLOCK DIAGRAM

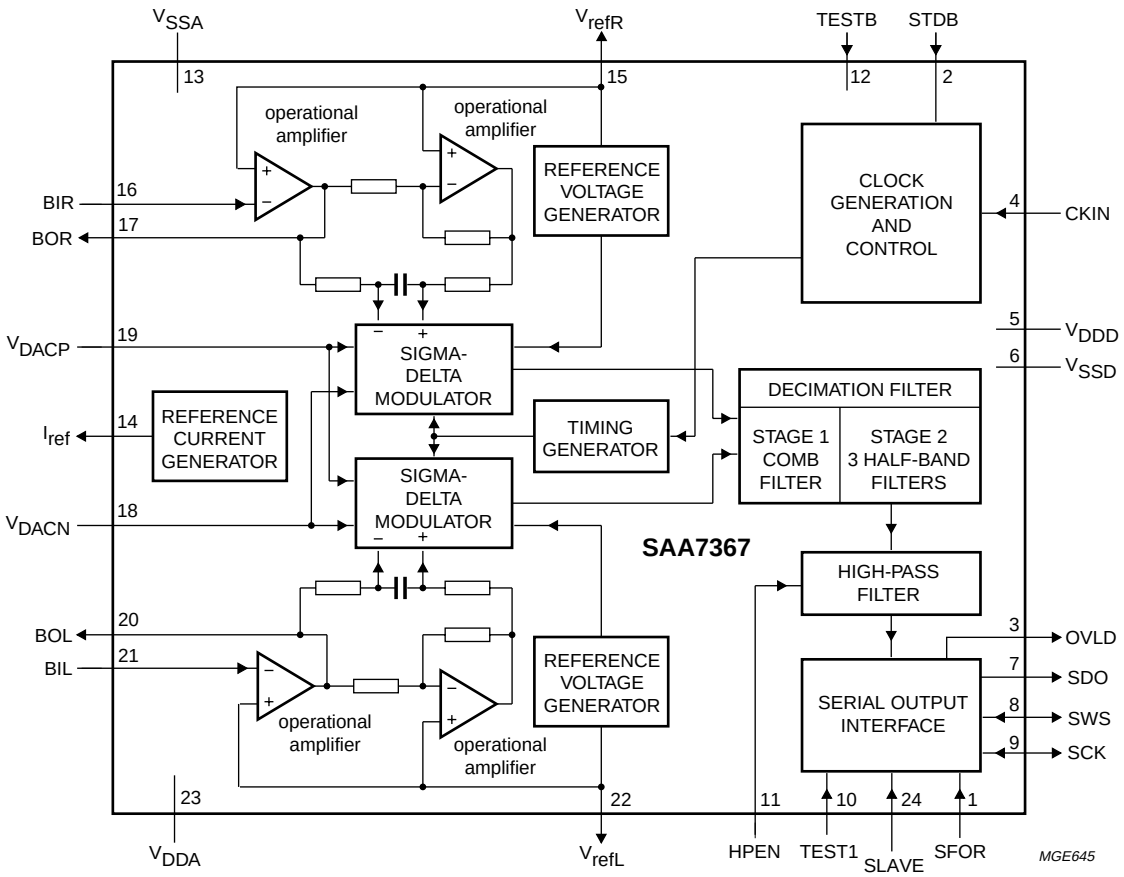


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SFOR	1	TTL level input; in normal mode this input selects the serial interface output format; output format is selected as follows: SFOR = HIGH selects Format 1 SFOR = LOW selects Format 2 (similar to I^2S)
STDB	2	schmitt-trigger input; in normal mode, this input is used to select standby mode:
		STDB = HIGH selects normal operation
		STDB = LOW selects standby mode (low power consumption)
OVLD	3	TTL level output; in normal mode this output indicates whether the internal digital signal is within 1 dB of maximum; if so, the output will go HIGH for 131072 clock cycles (approximately 11 ms); in standby mode this output is forced LOW
CKIN	4	CMOS level input; system clock input; nominally clocked at $256f_s$
V_{DDD}	5	digital supply voltage (4.5 to 5.5 V)
V_{SSD}	6	digital ground
SDO	7	TTL level output (3-state); in normal mode this pin outputs data from the serial interface; in standby mode, this output is high impedance
SWS	8	TTL level input/output; serial interface word select signal; in master mode (SLAVE = LOW), this pin outputs the serial interface word select signal; in slave mode (SLAVE = HIGH), this pin is the word select input to the serial interface; in standby mode (STDB = LOW) this pin is always an input (high impedance); for polarity: see Table 1
SCK	9	TTL level input/output; in master mode (SLAVE = LOW) the pin outputs the serial interface bit clock; in slave mode (SLAVE = HIGH) this pin is the input for the external bit clock; data on SDO is clocked out on the HIGH-to-LOW transition of SCK; the data is valid on the LOW-to-HIGH transition
TEST1	10	Test 1; TTL level input with internal pull-down; in slave mode (slave = HIGH), this pin is used to select extra serial interface formats (see Table 2)
HPEN	11	TTL level input; this input is used to enable the internal high-pass filter when HIGH; in scan-test mode (TESTB = LOW and TEST1 = LOW) this pin functions as ‘scan chain c’ input
TESTB	12	Test B; CMOS level input with internal pull-up; in normal applications, this input should be left HIGH
V_{SSA}	13	analog ground; this pin is internally connected to V_{SS} via the on-chip substrate contacts
I_{ref}	14	current reference generator output; 33 kΩ in parallel with 22 nF is connected from this pin to V_{SSA}
V_{refR}	15	right channel analog reference output voltage ($\frac{1}{2}V_{DDA}$)
BIR	16	buffer operational amplifier inverting input for right channel
BOR	17	buffer operational amplifier output for right channel
V_{DACN}	18	negative 1-bit DAC reference voltage input, connected to 0 V
V_{DACP}	19	positive 1-bit DAC reference voltage input, connected to +5 V
BOL	20	buffer operational amplifier output for left channel
BIL	21	buffer operational amplifier inverting input for left channel
V_{refL}	22	left channel analog reference output voltage ($\frac{1}{2}V_{DDA}$)
V_{DDA}	23	analog supply voltage (4.5 to 5.5 V)

SYMBOL	PIN	DESCRIPTION
SLAVE	24	TTL level input; used to select the serial interface operating mode: SLAVE = HIGH selects slave mode SLAVE = LOW selects master mode

Table 1 SWS polarity

CONDITIONS			POLARITY
SLAVE AND TEST1	SWS	SFOR	
SLAVE = LOW or TEST1 = LOW	LOW	LOW	left data
	LOW	HIGH	right data
SLAVE = HIGH and TEST1 = HIGH	LOW	LOW	right data
	LOW	HIGH	left data

Table 2 Selection of serial interface formats via TEST1

CONDITIONS		SELECTED FORMAT
SFOR	TEST1	
HIGH	LOW	format 1
	HIGH	format 2
LOW	LOW	format 3
	HIGH	format 4

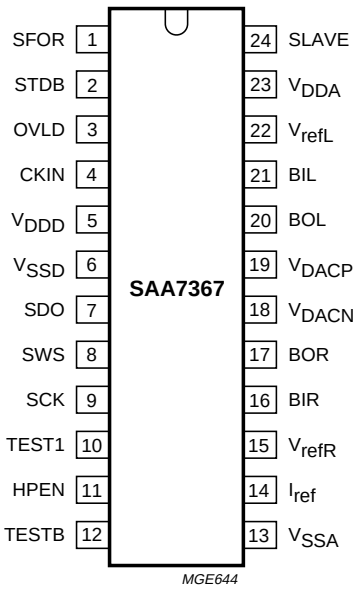


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

The SAA7367 is a bitstream conversion CMOS ADC for digital audio systems. The conversion is achieved using a third-order Sigma-Delta Modulator (SDM), running at 128 times the output sample frequency (f_s). The high oversampling ratio greatly simplifies the design of the analog input anti-alias filter. In most events, the internal buffer operational amplifier, configured as a low-pass filter, will suffice. The 1-bit code from the SDM is filtered and down-sampled (decimated) to $1f_s$ by Finite Impulse Response (FIR) filters. An optional I^2R high-pass filter is provided to remove DC, if required. The device has been designed with ease of use, low board area and low application costs in mind.

Clock frequency

The external clock input on pin CKIN runs at $256f_s$, which can range from 18 to 50 kHz.

Input buffer

Two input buffers are provided, one for each channel, for signal amplitude matching, signal buffering and anti-alias filter purposes. These are configured for inverting use. Access is provided by pins BIL, BIR (inverting inputs) and BOL, BOR (outputs), for left and right channels respectively. By the choice of feedback component values, the application signal amplitude can be matched to the requirements of the ADC.

Typically, the operational amplifiers are configured as low-pass filters with a gain of 1 and a pole at approximately $5f_s$.

Remark: the complete ADC is non-inverting. Hence, a positive DC input (referenced to V_{ref}) will yield a positive digital output.

Input level

The overall system gain is proportional V_{DDA}, or more accurately the potential difference between the DAC reference voltages (V_{VDACP}) and (V_{VDACN}). For convenience, the ADC input signal amplitude is defined as that amplitude seen on BOL or BOR, the operational amplifier outputs (i.e. the input to the SDM). Also, the 0 dB input level is defined as that which gives a –1 dB (actually –1.12 dB) digital output, relative to full-scale swing. This reduced gain provides headroom to accommodate small random DC offsets, without causing the digital output to clip.

Hence:

$$V_I(0\ dB) = \frac{(V_{VDACP} - V_{VDACN})}{5\ V\ (RMS)}$$

The user of the IC should ensure that, when all sources of signal amplitude variation are taken into account, the maximum input signal should conform to the 0 dB level. In the event that the maximum signal level cannot be pre-determined, e.g. live microphone input, the average signal level should be set at –10 to –20 dB down. The exact value will depend on the application and the balance between headroom and operating Signal-to-Noise Ratio (SNR).

Behaviour during overload

As previously defined, the maximum input level for normal operation is 0 dB. If the input level exceeds this value, clipping may occur. Within the system, excessive amplitudes are detected after the high-pass filter. Infringements are limited to the maximum permitted positive or negative values $2^{17} - 1$ or -2^{17} respectively.

Input signals in the range 0 to 1 dB may or may not be clipped, depending on the values of DC dither and small random offsets in the analog circuitry.

When using the recommended application circuitry, clipping will initially be observed on negative peaks, due to the use of negative DC dither.

The maximum level of overload that can be safely tolerated is application circuit dependent. In the case of the recommended circuit, the following applies: the inverting operational amplifier inputs BIL and BIR are protected from excessive voltages (currents) by diodes to V_{DDA} and V_{SSA}. These have absolute maximum ratings of $I_d = \pm 20$ mA, with a safe practical limit of ± 2 mA.

Given the input resistor of 10 kΩ, ±2 mA diode current and the operation of the operational amplifier, a maximum signal (applied to the input resistor) of ±30 V can be handled safely. This level represents an overload of 26 dB.

During overload, the in-band portion of the waveform will be correctly converted. The out-of-band portion will be limited as previously detailed.

Sigma-Delta Modulator (SDM)

The SAA7367 uses two third-order SDMs with a quantization noise floor of approximately –104 dB. The scaling of the feedback has been optimized for stable operation, even during overload. Thus, with a maximum signal swing of 0 V to V_{DDA} on the input, the digital output remains well-behaved, i.e. it does not burst into random oscillation. During overload, the output is simply a clipped version of the input. The gain of this stage is –4.64 dB.

Decimation filter

Decimation from $128f_s$ is performed in two stages. The first stage, a comb filter, uses 64 symmetrical coefficients to implement a 3rd sin x/x characteristic. This filter decimates from 128 to $8f_s$. The second stage, an FIR filter, consists of three half-band filters, each decimating by a factor of 2. The overall characteristics are given in Table 3.

Table 3 Overall filter characteristics

ITEM	CONDITION	VALUE (dB)
Pass band ripple	0 to $0.45f_s$	±0.1
	0.45 to $0.47f_s$	−0.5
Stop band	$>0.55f_s$	−60
Dynamic range	0 to $0.42f_s$	110
Gain	DC	3.52

High-pass filter

An optional I^2R high-pass filter is provided to remove unwanted DC components. The operation is selected when HPEN is HIGH and deselected when LOW. The filter has the characteristics given in Table 4.

Table 4 High-pass filter characteristics

ITEM	CONDITION	VALUE (dB)
Pass band ripple		none
Pass band gain		0
Droop	at $0.00042f_s$	0.146
Attenuation at DC	at $0.00000036f_s$	>40
Dynamic range	0 to $0.45f_s$	>110

Serial interface

The serial interface provides 2 formats in master mode and 4 in slave mode (see Figs 3 and 4). Format 2 is similar to Philips I^2S. In all modes, the interface provides up to 18 significant bits of output data per channel. During standby mode (STDB = LOW), all interface pins are in their high impedance state. On recovery from standby, the serial data output SDO is held LOW until valid data is available from the decimation filter. This time depends on whether the high-pass filter is selected:

HPEN = 0; T = $1024/f_s$, T = 21.3 ms when f_s = 48 kHz

HPEN = 1; T = $12288/f_s$, T = 256.0 ms when f_s = 48 kHz

Overload detection

The OVLD output is used to indicate when the output data, in either the left or right channel, is greater than −1 dB (actual figure −1.023 dB) of the maximum possible digital swing. When this condition is detected, the OVLD output is forced HIGH for at least $512f_s$ cycles (10.6 ms at f_s = 48 kHz). This time-out is reset for each infringement.

Standby mode

The STDB pin activates a power saving mode when the device function is not required. This pin can also be used as a chip enable.

On a HIGH-to-LOW transition of the STDB pin, the internal control circuitry starts a timed power-down sequence. This takes approximately 32 system clock cycles to complete. Transitions on STDB that are shorter than 32 clock cycles may have an indeterminate effect. However, the device will always recover correctly.

During standby, the following occurs:

- The internal logic clock is disabled
- The serial interface pins are forced to high impedance
- The OVLD output is forced LOW
- The analog circuitry is disabled
- The nominal external analog node voltages are maintained by a low-power circuit. This feature ensures a fast recovery from standby mode.

Note: since the serial interface pins are high impedance during standby, these pins could be wire-ORed with other serial interface ICs.

On a LOW-to-HIGH transition, the device reverts back to normal operation. This process takes approximately 256 system clock cycles. Before SDO is enabled, the output data is forced LOW. SDO remains LOW until good data is available from the decimation filter (see Section “Serial interface”).

The STDB pin has a Schmitt-trigger input. A simple power-on-reset function can be effected using an external capacitor to V_{SS} and resistor to V_{DD}.

TEST1

This pin is used to select the serial interface format in slave mode.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage (note 1)	–0.5	+6.5	V
V_I	DC input voltage	–0.5	+6.5	V
I_{IK}	DC input clamp diode current	–	±20	mA
V_O	DC output voltage	–0.5	V_{DD} + 0.5	V
I_O	DC output source or sink current	–	±20	mA
$I_{DD(tot)}$	total DC supply current	–	±0.5	A
I_{SStot}	total DC supply current	–	±0.5	A
T_{amb}	operating ambient temperature	–40	+85	°C
T_{stg}	storage temperature	–65	+150	°C

Note

1. V_{SSD} and V_{SSA} must be connected to a common potential.

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611-E"*. The number of the quality specification can be found in the *"Quality Reference Handbook"*. The handbook can be ordered using the code 9397 750 00192.

CHARACTERISTICS

V_{DDD} = 4.5 to 5.5 V; V_{DDA} = 4.5 to 5.5 V; f_s = 18 to 50 kHz; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDD}	digital supply voltage		4.5	5	5.5	V
I_{DDD}	digital supply current	f_s = 48 kHz	–	17	–	mA
V_{DDA}	analog supply voltage		4.5	5	5.5	V
I_{DDA}	analog supply current		–	13	–	mA
P_{tot}	total power dissipation	f_s = 48 kHz	–	150	–	mW
I_{stb}	standby supply current		–	160	–	µA
P_{stb}	standby power consumption		–	800	–	µW
Digital part: inputs						
SFOR, SLAVE AND HPEN						
V_{IL}	LOW level input voltage		–0.5	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current		–10	–	+10	µA
C_i	input capacitance		–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CKIN						
V_{IL}	LOW level input voltage		–0.5	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.5	V
I_{LI}	input leakage current		–10	–	+10	µA
C_i	input capacitance		–	–	10	pF
TEST1						
V_{IL}	LOW level input voltage		–0.5	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
R_i	internal resistance to V_{SS}		–	50	–	kΩ
C_i	input capacitance		–	–	10	pF
TESTB						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.5	V
R_i	internal resistance to V_{DD}		–	50	–	kΩ
STDB (SCHMITT TRIGGER)						
V_{IL}	LOW level input voltage		–0.5	–	$0.4V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.6V_{DD}$	–	V_{DD} + 0.5	V
V_{hys}	hysteresis voltage		200	–	–	mV
I_{LI}	input leakage current		–10	–	+10	µA
C_i	input capacitance		–	–	10	pF
Digital part: inputs/outputs						
SWS AND SCK						
V_{IL}	LOW level input voltage		–0.5	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0		V_{DD} + 0.5	V
I_{LI}	3-state leakage current		–10	–	+10	µA
C_i	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_O = –400 µA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = 20 µA	2.4	–	–	V
C_L	output load capacitance	note 1	–	–	50	pF
Digital part: outputs						
OVLD						
V_{OL}	LOW level output voltage	I_O = –400 µA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = 20 µA	2.4	–	–	V
C_L	output load capacitance	note 1	–	–	50	pF
SDO						
V_{OL}	LOW level output voltage	I_O = –400 µA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = 20 µA	2.4	–	–	V
I_{LI}	3-state leakage current		–10	–	+10	µA
C_L	output load capacitance	note 1	–	–	50	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital part: timings						
CKIN						
t_r	input rise time		–	–	10	ns
t_f	input fall time		–	–	10	ns
f_i	input frequency		4.60	–	12.8	MHz
msr	mark-to-space ratio	f_s > 32 kHz	40	–	60	%
		$f_s \leq$ 32 kHz	30	–	70	%
Serial Interface master and slave modes (see Figs 5 and 6)						
SCK						
t_r	rise time	C_L = 50 pF; note 1	–	–	50	ns
t_f	fall time	C_L = 50 pF; note 1	–	–	50	ns
t_L	LOW time	T = $\frac{1}{64}f_s$	0.4T	–	0.6T	ns
t_H	HIGH time	T = $\frac{1}{64}f_s$	0.4T	–	0.6T	ns
f_{clk}	clock frequency	master mode	$64f_s$	$64f_s$	$64f_s$	MHz
		slave mode	–	–	$64f_s$	MHz
t_{idle}	burst clock idle time	slave mode; T = $1/f_s$	0	–	0.5T	ns
SWS						
t_r	rise time	C_L = 50 pF; note 1	–	–	50	ns
t_f	fall time	C_L = 50 pF; note 1	–	–	50	ns
t_L	LOW time	T = $1/f_s$	0.05T	0.5T	0.95T	ns
t_H	HIGH time	T = $1/f_s$	0.05T	0.5T	0.95T	ns
f_S	frequency		$1f_s$	$1f_s$	$1f_s$	MHz
t_d	delay from SCK	master mode	–50	–	+50	ns
		slave mode	50	–		ns
t_{su}	set-up time to SCK	slave mode	150	–	–	ns
SDO						
t_h	data output hold time		100	–	–	ns
t_{su}	data output set-up time		50	–	–	ns
t_r	data output rise time	C_L = 50 pF; note 1	–	–	50	ns
t_f	data output fall time	C_L = 50 pF; note 1	–	–	50	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog part at: V_{DD} = V_{DDA} = 5 V; T_{amb} = 25 °C						
V_{refL} AND V_{refR}						
V_O	output voltage		$0.475V_{DDA}$	$0.5V_{DDA}$	$0.525V_{DDA}$	V
R_{DC}	DC impedance	normal mode	–	1.3	–	kΩ
		standby mode	–	100	–	kΩ
CURRENT REFERENCE: I_{ref}						
V_O	out put voltage		–	$0.5V_{DDA}$	–	V
I_O	output current	R = 33 kΩ	–	76	–	μA
V_{DACN}						
V_I	input voltage		–	V_{SS}	–	V
V_{DACP}						
V_I	input voltage		–	V_{DDA}	–	V
BUFFER OPERATIONAL AMPLIFIERS: BIL, BOL, BIR AND BOR						
$V_{I(off)}$	input offset voltage		–	<10	–	mV
R_L	load resistance; (drive capability)	decoupled to V_{ref}	–	10	–	kΩ
Z_O	output impedance		–	100	–	Ω
THD + N	total harmonic distortion plus noise	f = 0 to 20 kHz	–	–87	–	dB
OVERALL PERFORMANCE (ANALOG IN, DIGITAL OUT)						
t_{gd}	group delay time	T = $1/f_s$	–	25T	–	s
α_{sb}	stop band attenuation	f > 0.546 f_s	60	–	–	dB
DR	dynamic range	0 to 20 kHz	90	93	–	dB
THD + N	total harmonic distortion plus noise	0 to 20 kHz	–	–88	–80	dB
S/N	signal-to-noise ratio	A-weighted	–	97	–	dB
α_{cs}	channel separation		–	92	–	dB
G	gain	note 2	–1.4	–1	–0.8	dB

Notes

1. Load capacitance is valid for master mode only.
2. See also Section “Input level” of Chapter “Functional description”; valid for left or right channel.

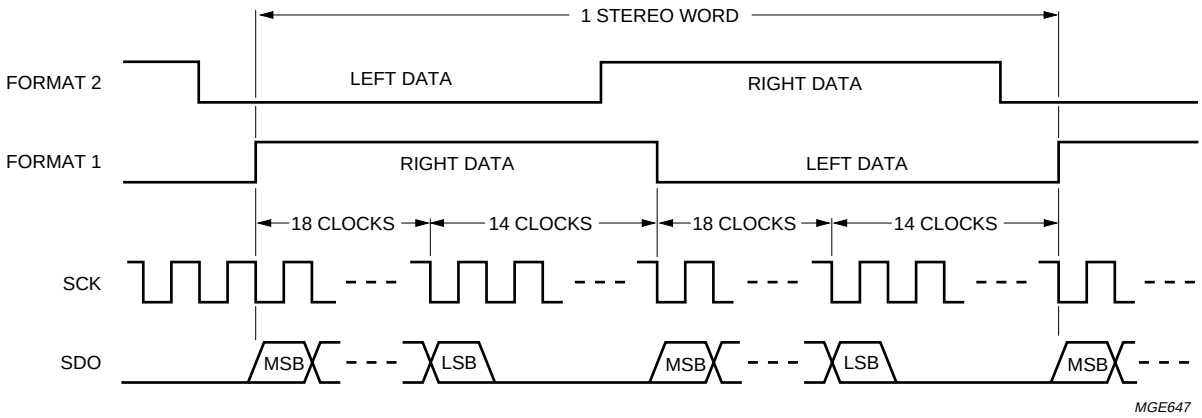


Fig.3 Serial interface master mode format.

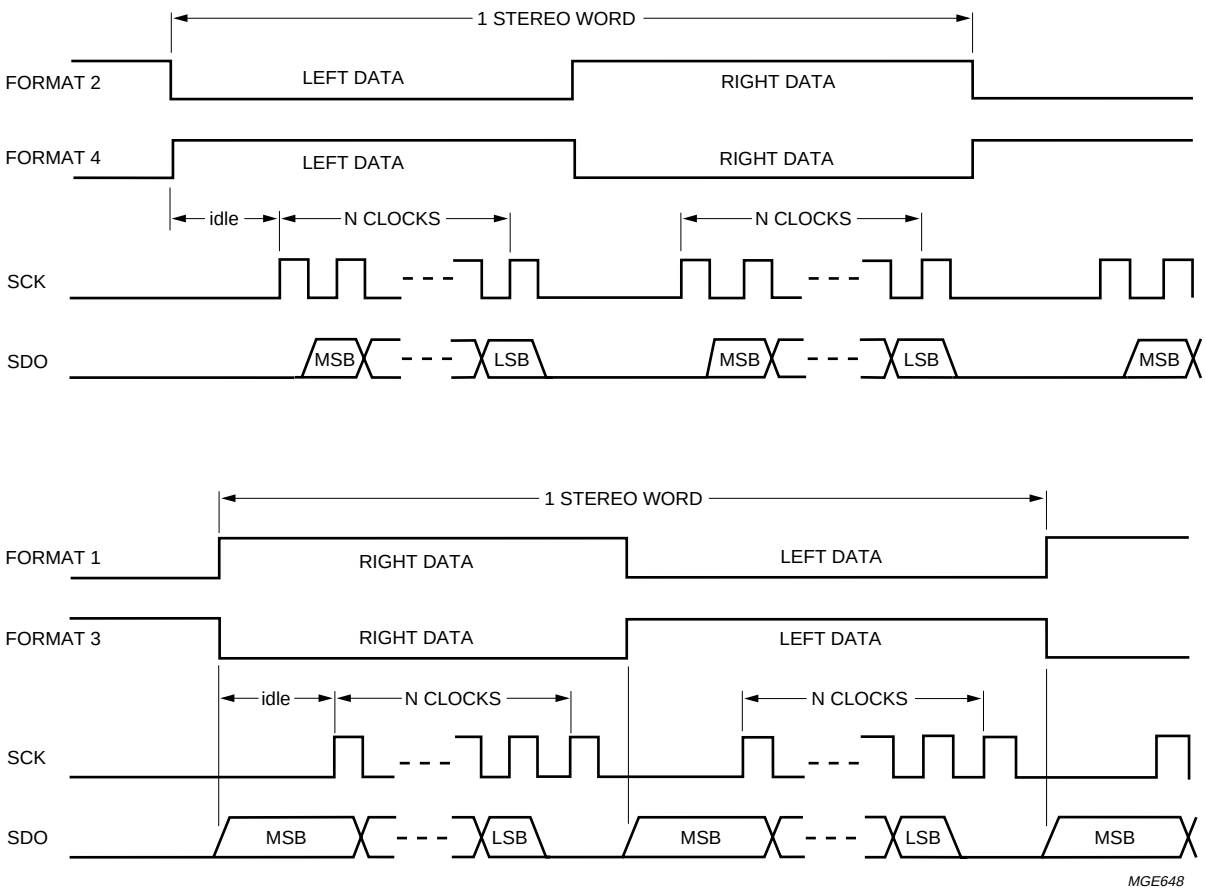


Fig.4 Serial interface slave mode format.

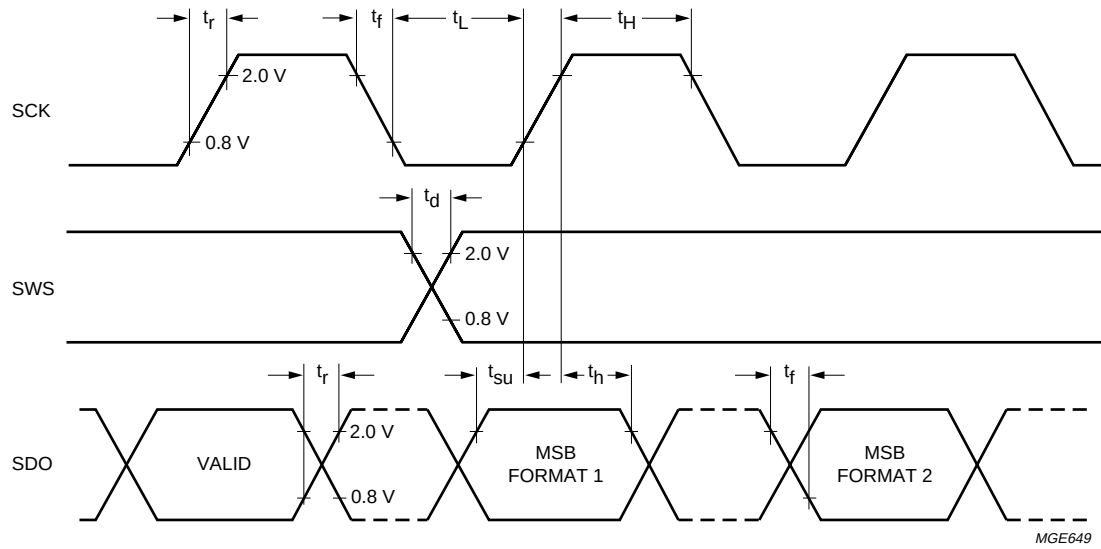


Fig.5 Serial interface master mode timing.

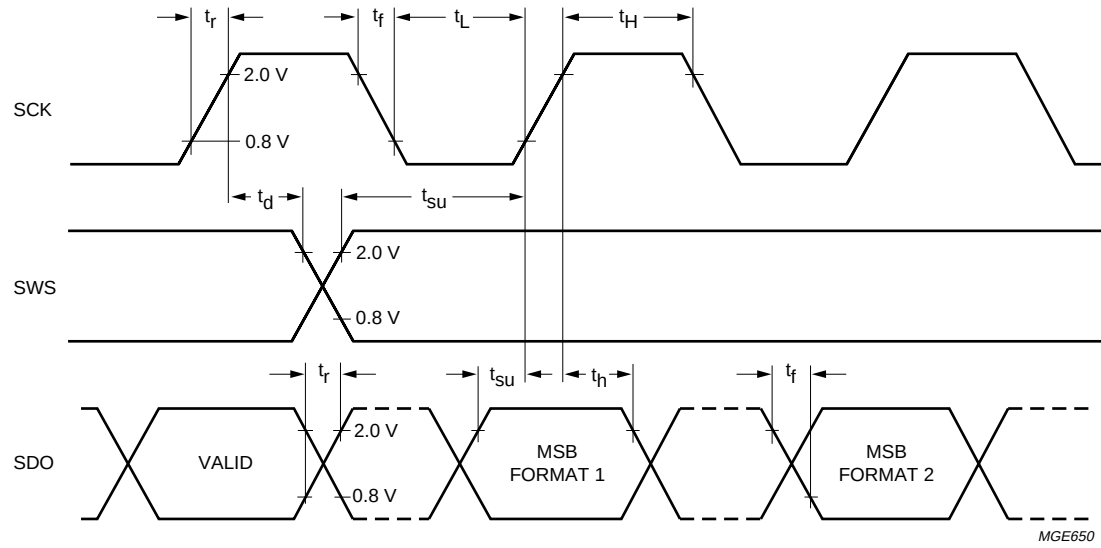
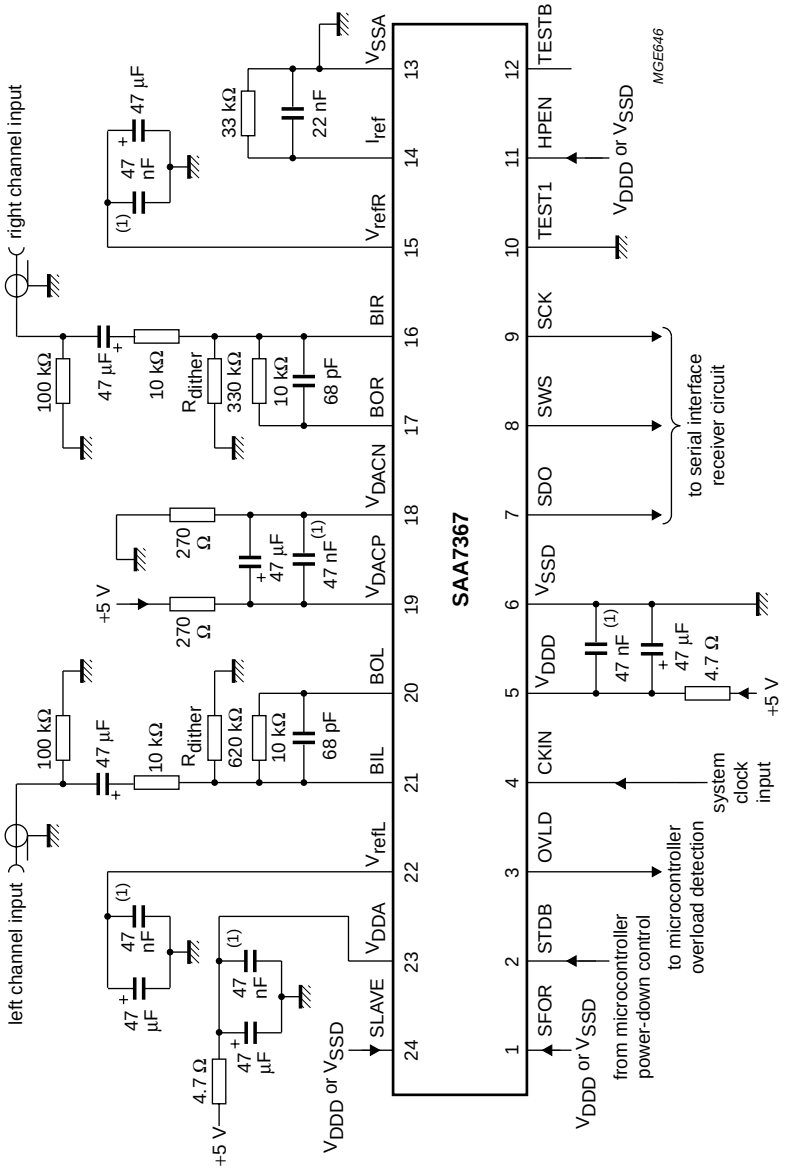


Fig.6 Serial interface slave mode timing.

APPLICATION INFORMATION

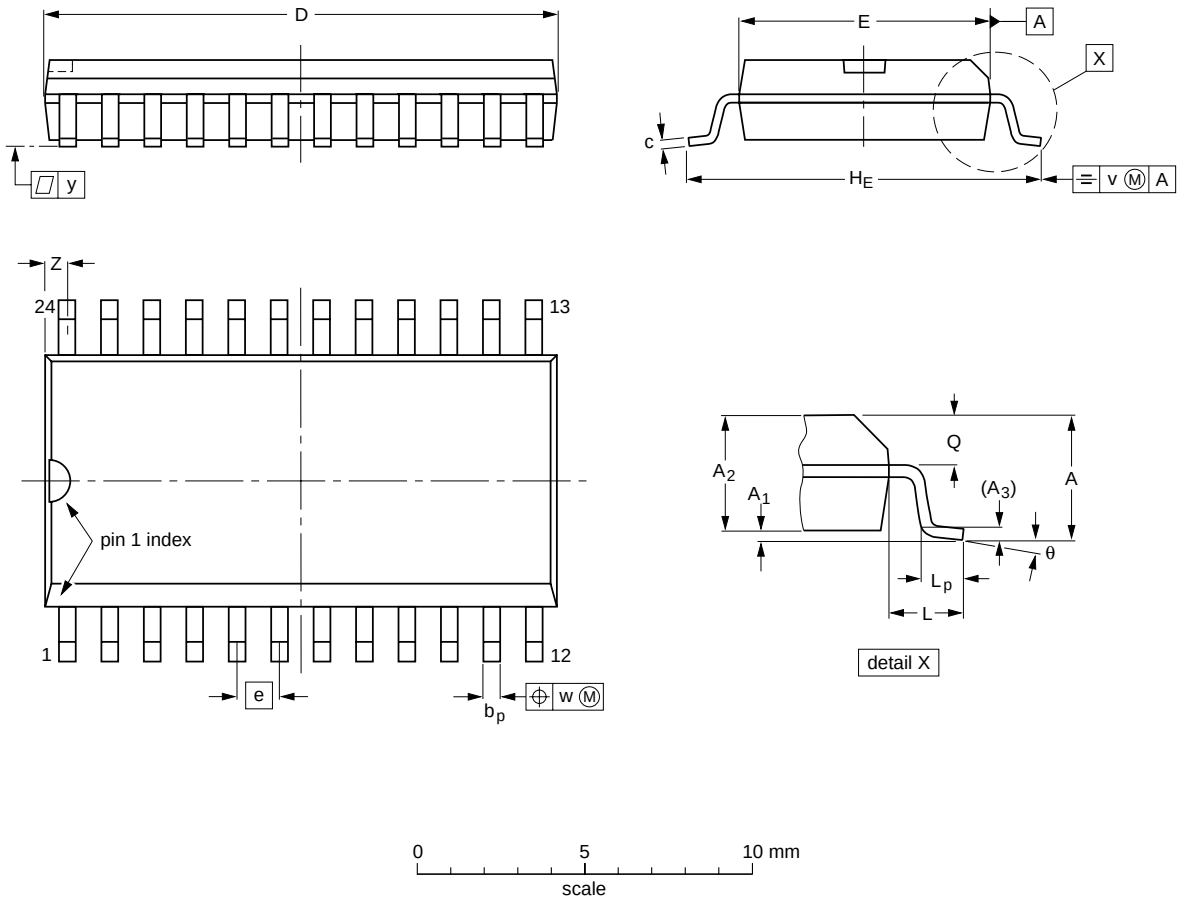


(1) These capacitors should preferably be surface-mounted components located as close as possible to the device pins.

Fig.7 Application circuit.

PACKAGE OUTLINE

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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